at least two or more two zener diodes connected in series comprised of:

a well region of a first conductivity type formed on said semiconductor substrate;

a first semiconductor region of said second conductivity type formed in said well region;

a second semiconductor region of said first conductivity type formed in said well region at a bottom portion of said first semiconductor region and being smaller in area, defined by a planar pattern thereof, than said first semiconductor region,

an insulation film formed over a primary face of said semiconductor substrate; and

C2 cont.

a plurality of first connection holes for electrically connecting therethrough said first semiconductor region and a plurality of second connection holes for electrically connecting therethrough said well region, both of which are formed in said insulation film;

wherein a wiring is formed over said insulation film and electrically connecting with said first connection holes of a first of said zener diodes and said second connection holes of a second of said zener diodes, said plurality of first connection holes, for electrically connecting said first semiconductor region and a wire to each other, are arranged in a region located outside a junction formed between said first semiconductor region and said second semiconductor region of said first zener diode, a first PN junction formed between said first semiconductor region and said second semiconductor region functions as a diode device, and a second PN junction is formed between said semiconductor

C2 cont.

substrate and said well region and has a breakdown voltage greater than that of said first PN junction .

C3

3. **(Amended)** A semiconductor integrated circuit device according to claim 1, wherein a junction depth of said first semiconductor region in a region in which said first and second semiconductor regions form a junction is shallower than that of said first semiconductor region in a region in which said well region and said first semiconductor region form a junction.

C4

22. **(Twice Amended)** A semiconductor integrated circuit device according to claim 2, wherein a junction depth of said first semiconductor region in a region in which said first and second semiconductor regions form a PN junction is shallower than that of said first semiconductor region in a region in which said well region and said first semiconductor region form a PN junction.

C5

24. **(Amended)** A semiconductor integrated circuit device according to claim 3, wherein said second semiconductor region has an impurity concentration higher than that of said well region.

C6

26. **(Amended)** A semiconductor integrated circuit device according to claim 1, wherein said second semiconductor region has an impurity concentration higher than that of said well region.

27. **(Amended)** A semiconductor integrated circuit device according to claim 22, wherein said second semiconductor region has an impurity concentration higher than that of said well region.

29. **(Amended)** A semiconductor integrated circuit device comprising:

a first diode and a second diode connecting in series, each of said first and second diode including:

a first semiconductor region of a first conductivity type being formed in a semiconductor substrate;

a second semiconductor region of a second conductivity type, the second semiconductor region being formed in said first semiconductor region;

a third semiconductor region of a first conductivity type, the third semiconductor region being formed in said first semiconductor region and under said second semiconductor region; and

an insulation film formed over a primary face of said semiconductor substrate; and

a plurality of first connection holes for electrically connecting therethrough said second semiconductor region and a plurality of second connection holes for electrically connecting therethrough said first semiconductor region, both of which are formed in said insulation film,

wherein a wiring is formed over said insulation film and electrically connecting said first connection holes associated with said first diode and said second connection holes associated with said second diode, a first PN junction formed between said second semiconductor region and said third semiconductor region functions as a diode device, said third semiconductor region has an

impurity concentration higher than that of said first semiconductor region, said second semiconductor region has a first portion and a second portion, the first portion is that in which a PN junction is formed between said third semiconductor region and said second semiconductor region and the second portion is that below which said third semiconductor region is not formed, a junction depth of said first portion is shallower than that of said second portion, said second portion is formed outside said first portion, and said first connection holes are formed over said second portion of said second semiconductor region.

32. **(Amended)** A semiconductor integrated circuit device comprising:

a first well region of a first conductivity type being formed in a semiconductor substrate;

a second well region of a second conductivity type being formed in said first well region;

a first semiconductor region of said first conductivity type, the first semiconductor region being formed in said second well region;

a second semiconductor region of said second conductivity type, the second semiconductor region being formed in said second well region under said first semiconductor region; and

an insulation film formed over a primary face of said semiconductor substrate and having a plurality of first connection holes for electrically connecting therethrough said first semiconductor region and wiring,

wherein said first semiconductor region has a first portion and a second portion, the first portion is that below which said second semiconductor region is formed and the second portion is that below which said second semiconductor

region is not formed, a first PN junction is formed between said second semiconductor region and said first semiconductor region at said first portion and functions as a diode device, said second portion is formed outside said first portion, said first connection holes are formed over said second portion of said first semiconductor region, and second semiconductor region has an impurity concentration higher than that of said second well region, and a second PN junction is formed between said first well region and said second well region and has a breakdown voltage greater than that of said first PN junction.

C8 cont.

36. **(Amended)** A semiconductor integrated circuit device comprising a first diode and a second diode connected in series and formed in a first well region, the first well region being formed on a semiconductor substrate, said first diode and said second diode, respectively, comprising:

a second well region of a first conductivity type, the second well region being formed in said first well region which is of a second conductivity type;

C9

a first semiconductor region of a second conductivity type, the first semiconductor region being formed in said second well region;

a second semiconductor region of a first conductivity type, the second semiconductor region being formed in said second well region and under said first semiconductor region; and

an insulation film formed over a primary face of said semiconductor substrate; and

a plurality of first connection holes for electrically connecting therethrough said first semiconductor region and a plurality of second connection holes for

electrically connecting therethrough said second well region, both of which are formed in said insulation film,

wherein a wiring formed on said insulation film and connection with said first connection holes in said first diode and said second connection holes in said second diode said second semiconductor region has an impurity concentration higher than that of said second well region, said first semiconductor region has a first portion and a second portion, the first portion is that below which said second semiconductor region is formed and the second portion is that below which said semiconductor region is not formed, a first PN junction is formed between said second semiconductor region and said first semiconductor region at said first portion and constitutes a zener diode, a junction depth of said first portion is shallower than that of said second portion, said second portion is formed in a periphery of said first portion so as to surround said first portion, said plurality of first connection holes are arranged over said second portion so as to surround said first portion, and a second PN junction is formed between said first well region and said second well region and has a breakdown voltage greater than that of said first PN junction.

C9 cont.

Please **insert** new claims 37 and 38, furthermore, as follows:

37. A semiconductor integrated circuit device according to claim 29, wherein a second PN junction is formed between said first semiconductor region and said semiconductor substrate and has a breakdown voltage greater than that of said first PN junction.

C10

38. A semiconductor integrated circuit device according to claim 29, said third semiconductor region has an impurity concentration higher than that of said first semiconductor region.

C 10 cont.